IN THE CLAIMS

Please cancel Claims 1-5, 8, 9, 12-17, 20, 21, 24, and 25 without prejudice or disclaimer.

Claims 1-5 (cancelled).

Claim 6 (currently amended): A clamping circuit ensuring that a voltage level at a node is within a specified range, said clamping circuit comprising:

a first transistor designed to be turned on when said voltage level is outside of said specified range;

a current amplifier drawing a substantial amount of current from said node when said first transistor is turned on, which causes said voltage level at said node to be pulled to within said specified range;

biasing circuit generating a bias signal to a gate terminal of said first transistor, wherein a voltage level of said bias signal is determined by an upper limit or a lower limit of said specified range; and

~~The clamping circuit of claim 4, wherein said current amplifier comprises:~~

a ~~third~~ second transistor and a ~~fourth~~ third transistor, wherein a gate terminal of said ~~fourth~~ third transistor is connected to a drain terminal of said ~~third~~ second transistor, a gate terminal of said ~~third~~ second transistor receiving a ~~third~~ second bias voltage, a source terminal of each of said ~~third~~ second transistor and said ~~fourth~~ third transistor is connected to ground, said drain terminal of said ~~third~~ second transistor is connected to a drain terminal of said first transistor, and a drain terminal of said ~~fourth~~ third transistor is connected to said source terminal of said first transistor.

Claim 7 (currently amended): The clamping circuit of claim 6, wherein each of said ~~third~~ second transistor and said ~~fourth~~ third transistor comprises a NMOS transistor.

Claims 8 and 9 (cancelled).

Claim 10 (currently amended): A clamping circuit ensuring that a voltage level at a node is within a specified range, said clamping circuit comprising:

a first transistor designed to be turned on when said voltage level is outside of said specified range;

a current amplifier drawing a substantial amount of current from said node when said first transistor is turned on, which causes said voltage level at said node to be pulled to within said specified range; and

biasing circuit generating a bias signal to a gate terminal of said first transistor, wherein a voltage level of said bias signal is determined by an upper limit or a lower limit of said specified range,

~~The clamping circuit of claim 4,~~ wherein said current amplifier comprises:

a ~~third~~ second transistor and a ~~fourth~~ third transistor, wherein a gate terminal of said ~~fourth~~ third transistor is connected to both drain and gate terminals of said ~~third~~ second transistor, a source terminal of said ~~fourth~~ third transistor is connected to ground, said drain terminal of said ~~third~~ second transistor is connected to a drain terminal of said first transistor, and a drain terminal of said ~~fourth~~ third transistor is connected to a source terminal of said first transistor; and

a resistor connected between a source terminal of said ~~third~~ second transistor and ground.

Claim 11 (currently amended): The clamping circuit of claim 10, wherein each of said ~~third~~ second transistor and said ~~fourth~~ third transistor comprises a NMOS transistor.

Claims 12-17 (cancelled).

Claim 18 (currently amended): A device comprising:

a clamping circuit ensuring that a voltage level at a node is within a specified range, said clamping circuit comprising:

a first transistor designed to be turned on when said voltage level is outside of said specified range; and

a current amplifier drawing a substantial amount of current from said node when said first transistor is turned on, which causes said voltage level at said node to be pulled to within said specified range,

wherein said clamping circuit further comprises a biasing circuit generating a bias signal to a gate terminal of said first transistor, wherein a voltage level of said bias signal is determined by an upper limit or a lower limit of said specified range, and

~~The device of claim 16,~~ wherein said current amplifier comprises:

a ~~third~~ second transistor and a ~~fourth~~ third transistor, wherein a gate terminal of said ~~fourth~~ third transistor is connected to a drain terminal of said ~~third~~ second transistor, a gate terminal of said ~~third~~ second transistor receiving a ~~third~~ second bias voltage, a source terminal of each of said ~~third~~ second transistor and said ~~fourth~~ third transistor is connected to ground, said drain terminal of said ~~third~~ second transistor is connected to a drain terminal of said first transistor, and a drain terminal of said ~~fourth~~ third transistor is connected to said source terminal of said first transistor.

Claim 19 (currently amended): The device of claim 18, wherein each of said ~~third~~ second transistor and said ~~fourth~~ third transistor comprises a NMOS transistor.

Claims 20-21 (cancelled).

Claim 22 (currently amended): A device comprising:

a clamping circuit ensuring that a voltage level at a node is within a specified range, said clamping circuit comprising:

a first transistor designed to be turned on when said voltage level is outside of said specified range; and

a current amplifier drawing a substantial amount of current from said node when said first transistor is turned on, which causes said voltage level at said node to be pulled to within said specified range,

wherein said clamping circuit further comprises a biasing circuit generating a bias signal to a gate terminal of said first transistor, wherein a voltage level of said bias signal is determined by an upper limit or a lower limit of said specified range, and

~~The device of claim 16,~~ wherein said current amplifier comprises:

a ~~third~~ second transistor and a ~~fourth~~ third transistor, wherein a gate terminal of said ~~fourth~~ third transistor is connected to both drain and gate terminals of said ~~third~~ second transistor, a source terminal of said ~~fourth~~ third transistor is connected to ground, said drain terminal of said ~~third~~ second transistor is connected to a drain terminal of said first transistor, and a drain terminal of said ~~fourth~~ third transistor is connected to a source terminal of said first transistor; and

a resistor connected between a source terminal of said ~~third~~ second transistor and ground.

Claim 23 (currently amended): The device of claim 22, wherein each of said ~~third~~ second transistor and said ~~fourth~~ third transistor comprises a NMOS transistor.

Claims 24 and 25 (cancelled).